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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/687,838	10/20/2003	Jung-Hwan Oh	SEC.926D	2012

7590 08/02/2004

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EXAMINER	
NGUYEN, DAO H	
ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 08/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/687,838	OH ET AL.	
	Examiner	Art Unit	
	Dao H Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1003, 0304 & 0404*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. In response to the communications dated 10/20/2003 through 04/28/2004, claims 1-32 are active in this application as a result of the cancellation of claims 33-36 in the Preliminary Amendment.

Acknowledges

2. Receipt is acknowledged of the following items from the Applicant.

a. Information Disclosure Statement (IDS) filed on 10/20/2003, 10/29/2003, 03/26/2004, 03/31/2004 and 04/28/2004. The references cited on the PTOL 1449 form have been considered.

Applicant is requested to cite any relevant prior art if being aware on form PTO-1449 in accordance with the guidelines set for in M.P.E.P. 609.

b. This application is a Divisional of the co-pending Application Serial No. 10/136,385 filed 05/02/2002, now patent No. 6,700,153.

Specification

3. The specification is objected to for the following reason: In the specification, page 11, lines 13 and 15, the reference number "155" should be changed to "115" in order to be consistent with the drawings.

4. The specification has been checked to the extent necessary to determine the presence of possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

5. Claim 1 and 17 are objected to because of the following reasons:

In claim 1, lines 15-16, and claim 17, lines 18-19, the word "at" in the phrase "so **at** to expose a surface portion of the etch stop layer" should be changed to –as--.

Claim Rejections - 35 U.S.C. § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim(s) 1-32 is/are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,215,187 to Ooto et al., in view of Jeng et al., U.S. Patent No. 6,136,643.

Regarding claims 1 and 17, Ooto discloses a method of fabricating a capacitor, comprising forming a lower electrode 8 over and interlayer insulating layer 5c, forming a dielectric layer 1 over the lower electrode 8, and forming an upper electrode 9 over the dielectric layer 1, as shown in figures 2-18, wherein the method of fabricating the lower capacitor electrode 8 comprising:

forming a lower mold layer 5d over a surface of a conductive plug 7 extending at a depth from the surface of the interlayer insulating layer 5c, and adjusting a wet etch rate of the lower mold layer 5d by adding dopants to the lower mold layer during formation of the lower mold layer, and by annealing the lower mold layer (column 10, lines 44-49);

forming an upper mold layer 5e over the surface of the lower mold layer 5d, wherein a wet etch rate of the upper mold layer 5e is less than the adjusted wet etch rate of the lower mold layer 5d (column 10, lines 47-47),

dry etching the upper mold layer 5e, and the lower mold layer 5d to form an opening 50 therein which exposes at least a portion of the surface of the contact plug 7;

wet etching the upper mold layer 5e and the lower mold layer 5d so as to increase a size of the opening at the lower mold layer 5d; and

depositing a conductive material 8 over the surface of the opening 51 in the upper and lower mold layers, and an exposed surface of the conductive plug 7. See figs. 1-9, and column 10, lines 44-65.

Ooto does not discuss about forming an etch stop layer over a surface of the interlayer insulating layer and over a surface of the conductive plug; and wet etching the mold layers so as to expose a surface portion of the etch stop layer adjacent the surface of the conductive plug.

However, Jeng discloses a method of fabricating a capacitor electrode, as shown in figures 11-13, comprising an etch stop layer 32 over a surface of the interlayer insulating layer 22/26 and over a surface of the conductive plug 24; and etching the layer 36 so as to expose a surface portion of the etch stop layer 32 adjacent the surface of the conductive plug 24.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Ooto so that it would include an etch stop layer as that of Jeng in order to prevent over etching (see the abstract of Jeng).

It is also noted that forming an etch stop layer to prevent over etching in forming a capacitor electrode is very well known in the art (see U.S. Patent No 5,545,585 for example).

Regarding claim 2, Ooto/Jeng discloses the method further comprising removing the upper and lower mold layers after depositing the conductive material. See figs. 13 of Jeng.

Regarding claim 18, Ooto discloses the method comprising all claimed limitation, except for removing a portion of the insulating layer deposited over the conductive material, and the conductive material to expose the upper mold layer; and removing a remaining portion of the insulating layer and the upper and lower mold layers.

Jeng discloses the method comprising depositing an insulating layer 42 over the conductive material 40 and within the opening; removing a portion of the insulating layer 42 and the conductive material 40 to expose the upper mold layer; and removing a remaining portion of the insulating layer 42 and the upper and lower mold layers 40. See figs. 12-13, and column 7, line 54 to column 8, line 10.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Ooto so that it would include the step of removing a portion of the insulating layer and the conductive material to expose the upper mold layer and then removing the remaining portion of the insulating layer and the upper mold layers as that of Jeng in order to prevent etching of the conducting layer in the opening. See column 7, lines 59-64 of Jeng.

Regarding claims 3-15 and 19-31, Ooto/Jeng discloses the methods comprising all claimed limitations. Note that selecting a known material or a known deposition method on the basis of its suitability for the intended use as a matter of obvious design choice; or discovering the optimum or working ranges involves only routine skill in the art. See column 10, lines 11 to column 12, line 33 of Ooto. See also column 4, lines 52 to column 7, line 67 of Jeng.

Regarding claims 16 and 32, Ooto/Jeng discloses the method wherein the conductive material 8 forms a cylindrical electrode defined by a cylindrical wall and a bottom wall which extends over a surface of the conductive plug 7, wherein the cylindrical wall extends upwardly from the bottom wall away from the surface of the interlayer insulating layer;

wherein the cylindrical wall of the cylindrical electrode 8 is defined by an upper cylindrical wall portion (formed in upper mold layer 5e), a lower cylindrical wall portion (formed in lower mold layer 5d), and an intermediate cylindrical wall portion located between the upper and lower cylindrical wall portions;

wherein a diameter of the upper cylindrical wall portion and a diameter of the lower cylindrical wall portion increase with an increase in a distance from the surface of the bottom wall, wherein a diameter of the intermediate cylindrical wall portions decreases with an increase in a distance away from the surface of the bottom wall, and wherein

$$A \geq C,\ C > B, \text{ and } C > D$$

where A is a diameter of the upper cylindrical wall portion at a location farthest from the bottom wall, B is a diameter of the upper cylindrical wall portion at a location nearest to the bottom wall, C is a diameter of the lower cylindrical wall portion at a location farthest from the bottom wall, and D is a diameter of the lower cylindrical wall portion at the bottom wall. See figs. 1, and 7-9 of Ooto.

Conclusion

8. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao H. Nguyen whose telephone number is (571)272-1791. The examiner can normally be reached on Monday-Friday, 9:00 AM – 6:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571)272-1787. The fax numbers for all communication(s) is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-1625.

David Nelms
Supervisory Patent Examiner
Technology Center 2800

Dao H. Nguyen
Art Unit 2818
July 27, 2004